

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/489954

Filing Date: January 24, 2000

Title: METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

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IN THE CLAIMS

Please amend the claims as follows:

1-39. (Canceled)

40. (Currently Amended) The electrode as specified in ~~Claim 39~~ Claim 44, wherein said second portion and said third portion are different materials.

41. (Previously Presented) The electrode as specified in Claim 40, wherein the said first portion and the said third portion are different materials.

42-43. (Canceled)

44. (Currently Amended) ~~The electrode as specified in Claim 39,~~ An electrode comprising:

- a) a first portion formed in an insulative layer having an upper surface;
- b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and
- c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials, wherein said first portion is a silicon contact.

45. (Currently Amended) ~~The electrode as specified in Claim 39,~~ An electrode comprising:

- a) a first portion formed in an insulative layer having an upper surface;
- b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and

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c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials, wherein said second portion is a diffusion barrier layer prohibiting diffusion of atoms between said first and said third portions.

46. (Currently Amended) An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and

c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials, wherein said third portion is an oxidation resistant layer.

47. (Currently Amended) The electrode as specified in ~~Claim 39~~ Claim 46, wherein said insulative layer surrounds a lower sidewall of said third portion.

48-51. (Canceled)

52. (Currently Amended) The dynamic random access memory device as specified in ~~Claim 54~~ claim 54, wherein said second portion and said third portion are different materials.

53. (Previously Presented) The dynamic random access memory device as specified in Claim 52, wherein said first portion and said third portion are different materials.

54. (Currently Amended) ~~The dynamic random access memory device as specified in Claim 51, further comprising~~ A dynamic random access memory device comprising:
a capacitor including an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

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b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above said upper surface;

c) a third portion overlying said second portion and, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion are different materials;

[[a)] d) a dielectric layer overlying said third portion; and

[[b)] e) a cell plate electrode overlying said dielectric layer.

55. (Currently Amended) The dynamic random access memory device as specified in ~~Claim 51~~ claim 54 further comprising a transistor.

56. (Previously Presented) An electrode comprising:

a) a contact formed in an insulative layer having an upper surface;

b) a diffusion barrier portion overlying said contact, said insulative layer surrounding a sidewall of said diffusion barrier portion and said diffusion barrier portion not extending above said upper surface ; and

c) an oxidation resistant portion overlying said diffusion barrier portion and, extending above and below said upper surface of said insulative layer, and including a recess, said diffusion barrier portion configured to inhibit diffusion of atoms between said contact and said oxidation resistant portion.

57-87. (Canceled)

88. (Previously Presented) An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion and said second portion does not extend above the upper surface; and

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c) a third portion overlying said second portion, extending above and below said upper surface of said insulative layer, and including a recess, wherein said first portion and said second portion respectively consist essentially of polysilicon and tantalum.

89. (Previously Presented) The electrode as specified in Claim 88, wherein said third portion consist essentially of platinum.

90-93. (Canceled)

94. (Currently Amended) The electrode of ~~Claim 93~~ Claim 95, wherein the second portion and the third portion are different materials.

95. (Currently Amended) ~~The electrode of Claim 93, wherein~~ An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface; and

c) a third portion overlying the second portion, extending above and below the upper surface of the insulative layer, and including a recess, wherein the first portion and the second portion are different materials and the first portion is a silicon contact.

96. (Currently Amended) The electrode of ~~Claim 93~~ Claim 95, wherein the second portion is a diffusion barrier layer.

97. (Currently Amended) ~~The electrode of Claim 93, wherein~~ An electrode comprising:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface; and

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c) a third portion overlying the second portion, extending above and below the upper surface of the insulative layer, and including a recess, wherein the first portion and the second portion are different materials and the third portion is an oxidation resistant layer.

98. (Currently Amended) The electrode of ~~Claim 93~~ Claim 97, wherein the insulative layer surrounds a sidewall of the third portion.

99. (Currently Amended) The electrode of ~~Claim 93~~ Claim 97, wherein the insulative layer surrounds the sidewall of the second portion.

100-105. (Canceled)

106. (Currently Amended) The dynamic random access memory device as specified in ~~Claim 105~~ Claim 108, wherein the second portion and the third portion are different materials.

107. (Currently Amended) The dynamic random access memory device as specified in ~~Claim 105~~ Claim 108, wherein the first portion and the third portion are different materials.

108. (Currently Amended) ~~The dynamic random access memory device as specified in Claim 105, further comprising:~~ A dynamic random access memory device comprising:
a capacitor including an electrode which comprises:

a) a first portion formed in an insulative layer having an upper surface;

b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface, wherein the first portion and the second portion are different materials;

c) a third portion overlying the second portion and, extending above and below the upper surface of the insulative layer, and including a recess; and

[[a)] d) a dielectric layer overlying the third portion; and

[[b)] e) a cell plate electrode overlying the dielectric layer.

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109. (Currently Amended) The dynamic random access memory device as specified in ~~Claim 105~~ Claim 108 further comprising a transistor.

110. (Currently Amended) The electrode of Claim 105, wherein the first portion contacts the second portion, and the second portion contacts the third portion.

111. (Currently Amended) The electrode of ~~Claim 105~~ Claim 108, wherein the insulative layer surrounds the sidewall of the second portion.

112. (Previously Presented) An electrode comprising:

- a) a contact formed in an insulative layer having an upper surface;
- b) a diffusion barrier portion overlying the contact and having a sidewall substantially flush with the upper surface; and
- c) an oxidation resistant portion overlying the diffusion barrier portion and extending above and below the upper surface, and including a recess, the diffusion barrier portion configured to inhibit diffusion of atoms between the contact and the oxidation resistant portion.

113. (Previously Presented) The electrode of Claim 112, wherein the contact contacts the diffusion barrier portion, and the diffusion barrier portion contacts the oxidation resistant portion.

114. (Previously Presented) An electrode comprising:

- a) a first portion formed in an insulative layer having an upper surface;
- b) a second portion overlying the first portion and having a sidewall substantially flush with the upper surface;
- c) a third portion overlying the second portion, extending above and below the upper surface, and including a recess, wherein the first portion and the second portion respectively consist essentially of polysilicon and tantalum.

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115. (Previously Presented) The electrode as specified in Claim 114, wherein the third portion consist essentially of platinum.

116. (Previously Presented) The electrode of Claim 114, wherein the first portion contacts the second portion, and the second portion contacts the third portion.